EuroPAT MASiP

EFECS 2020 virtual event
25-26.11.2020

Project presentation

ECSEL Joint Undertaking

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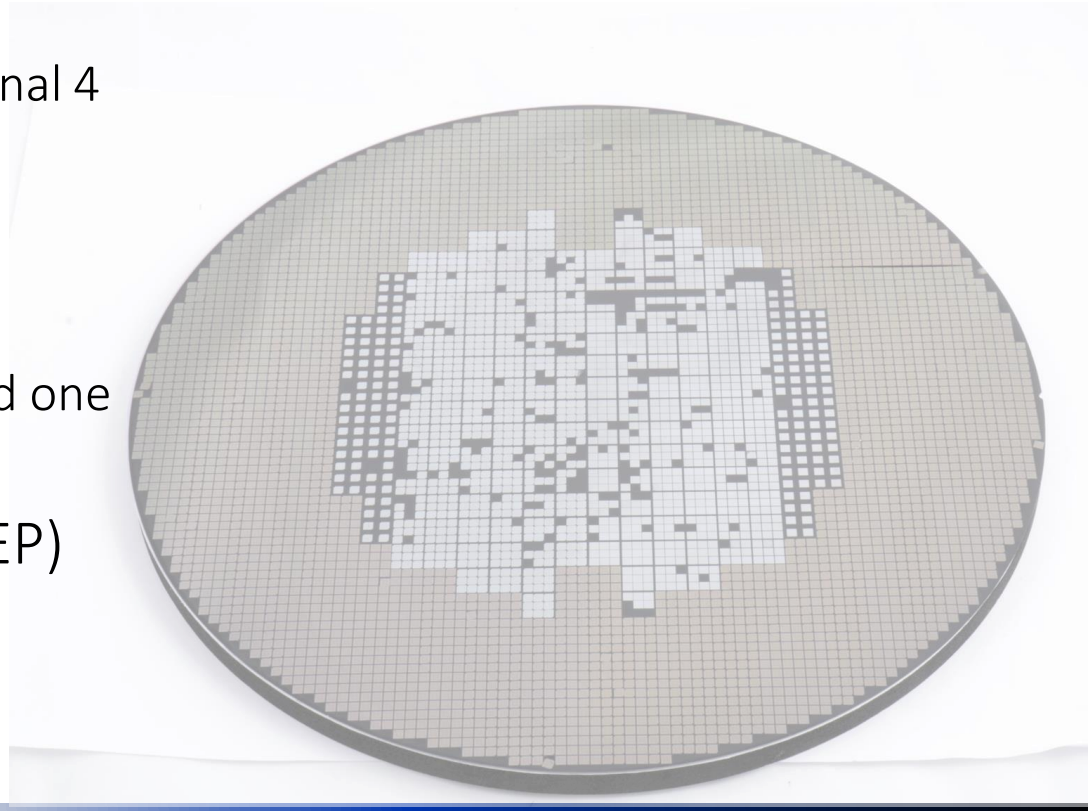
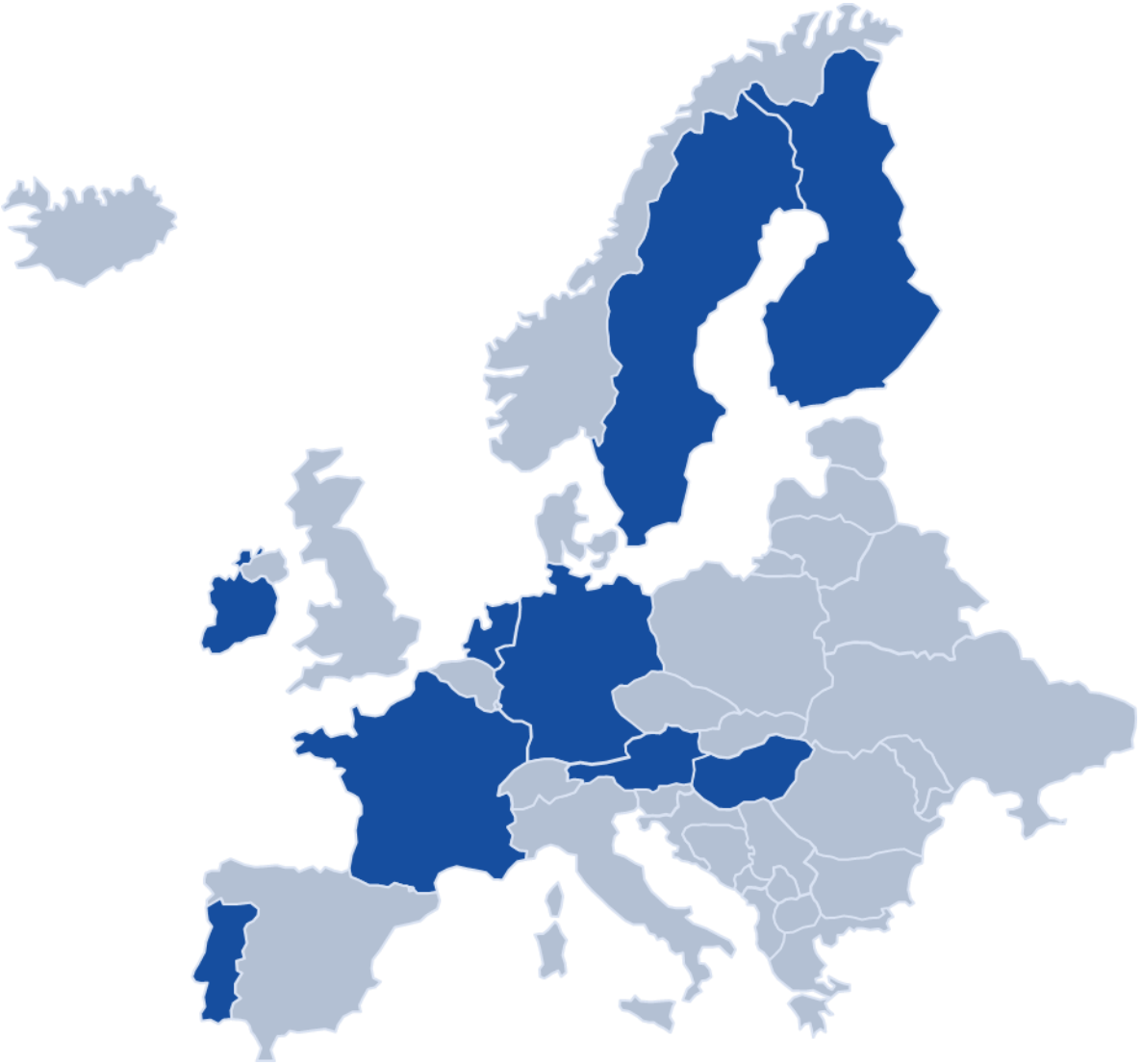
European Packaging, Assembly and Test Pilot for Manufacturing of Advanced System-In-Package (EuroPAT-MASIP)

- Originally 3-year project
  - started in April 2017
  - 2 extension periods of 9+6 months → altogether additional 4 years & 3 months
  - ends in June 2021
- ECSEL project with a total budget of about 30 M€
  - roughly one half of the funding comes from ECSEL JU and one half from national funding
- Coordinated by Amkor Technologies Portugal (ATEP)



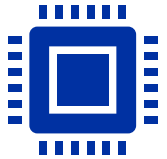
EuroPAT-MASIP consortium

- 28 partners from 9 European countries



EuroPAT-MASIP is...

- Increasing the competitiveness of the European semiconductor industry
  - The focus of the project is to **accelerate the manufacturing uptake of advanced packaging technologies and shorten the time-to-market**

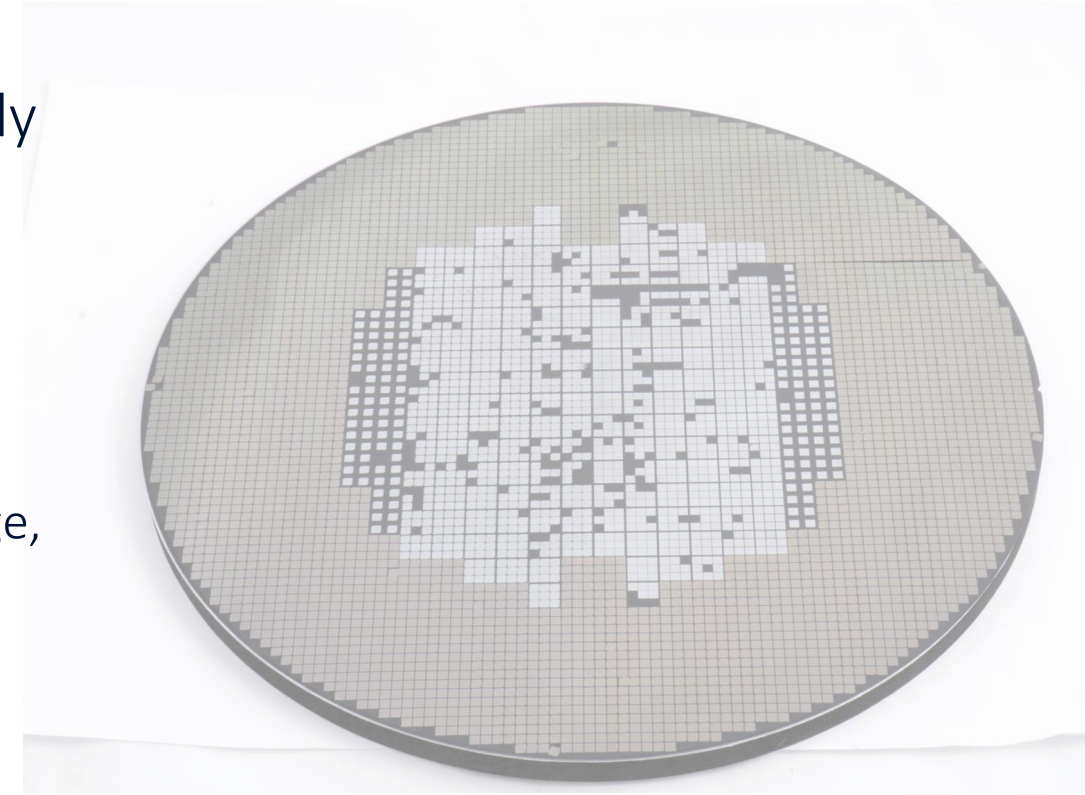


- Taking the whole value chain onboard
  - Each application pilot is built by several partners, including research institutes, SMEs and large companies → **building a European semiconductor ecosystem!**

- Challenging the existing practises in packaging
  - **Miniaturization** through densely packed System-in-Package, Sensor and MEMS integration

EuroPAT-MASIP scope

Further development and application of several leading-edge advanced packaging technologies, mainly **Fan-Out Wafer-Level Packaging (FO-WLP/WLFO)** and Embedding Technologies towards **2D and 3D System Integration**



- Miniaturization through densely packed System-in-Package, Sensor and MEMS integration, manufacturable in volume production at high yield and reasonable cost
- Study and consideration of Chip-Package-Interaction (CPI) and Chip-Board-Interaction (CBI) effects at the interface between the chip and the package/ system

Objectives of EuroPAT-MASiP Project

EuroPAT-MASiP **will develop**

Modelling, design and simulation of packaging-related key features and challenges

Test strategy, including metrology, methods and equipment, reliability and failure analysis

Heterogeneous (3D) integration of the smart system building blocks

More than Moore (MtM)

System in Package (SiP)

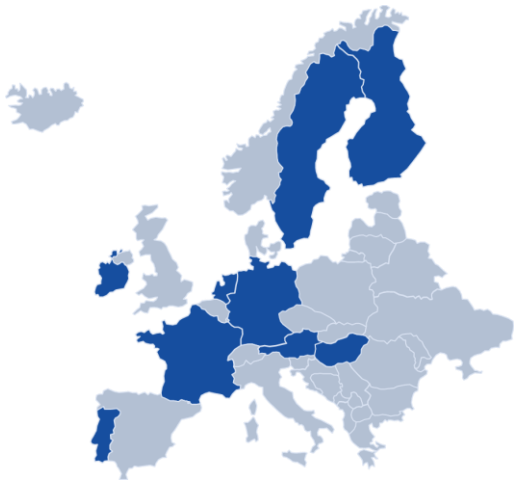
The key packaging technologies, equipment and materials

High Level Objectives

Boost Advanced Packaging Business in Europe

By 2022, the industrial partners involved will see:

- Increased turnover by 150 M€
- Increased market share, secured market leadership
- 280 new jobs
- Investments of 25 M€

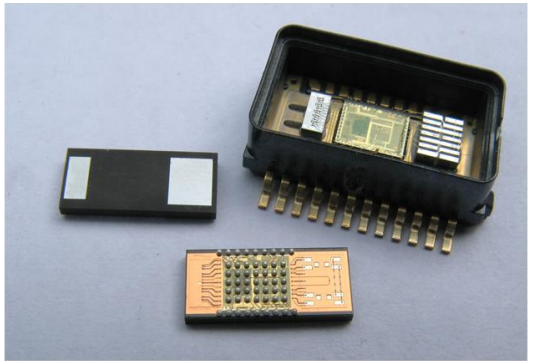


European Manufacturing Competitiveness enabled by

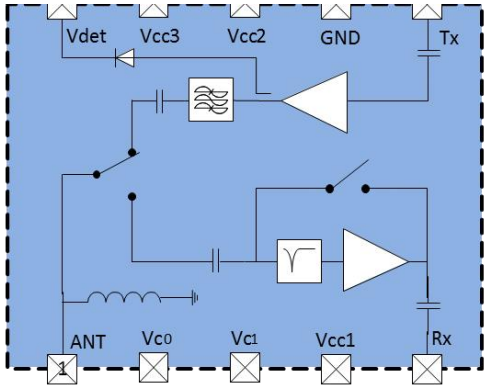
- Virtual Prototyping - Simulation Models for 'First time right' capability
- Process development addressing current limitations
- System Integration Concepts for automotive and industrial products
- Proof of manufacturability in volume production at high yield
- Development of test concepts and test equipment platform

Advanced packaging solutions will be validated in 6 Application Pilots

- **AP#1**: Automotive combined inertial sensor system
- **AP#2**: Intelligent car tyre sensor
- **AP#3**: High-performance camera module for automotive applications
- **AP#4**: Silicon photomultiplier with new packaging technology
- **AP#5**: High-frequency radar chipset (60 GHz / 77 GHz)
- **AP#6**: WLAN front-end IC with 3D packaging



MuRata automotive inertial combo-sensor.



Fully integrated RF front-end concept

Applications for high-frequency, high-performance and low-cost radars: door openers, industrial, traffic monitoring and survey/security.

An example of new test design

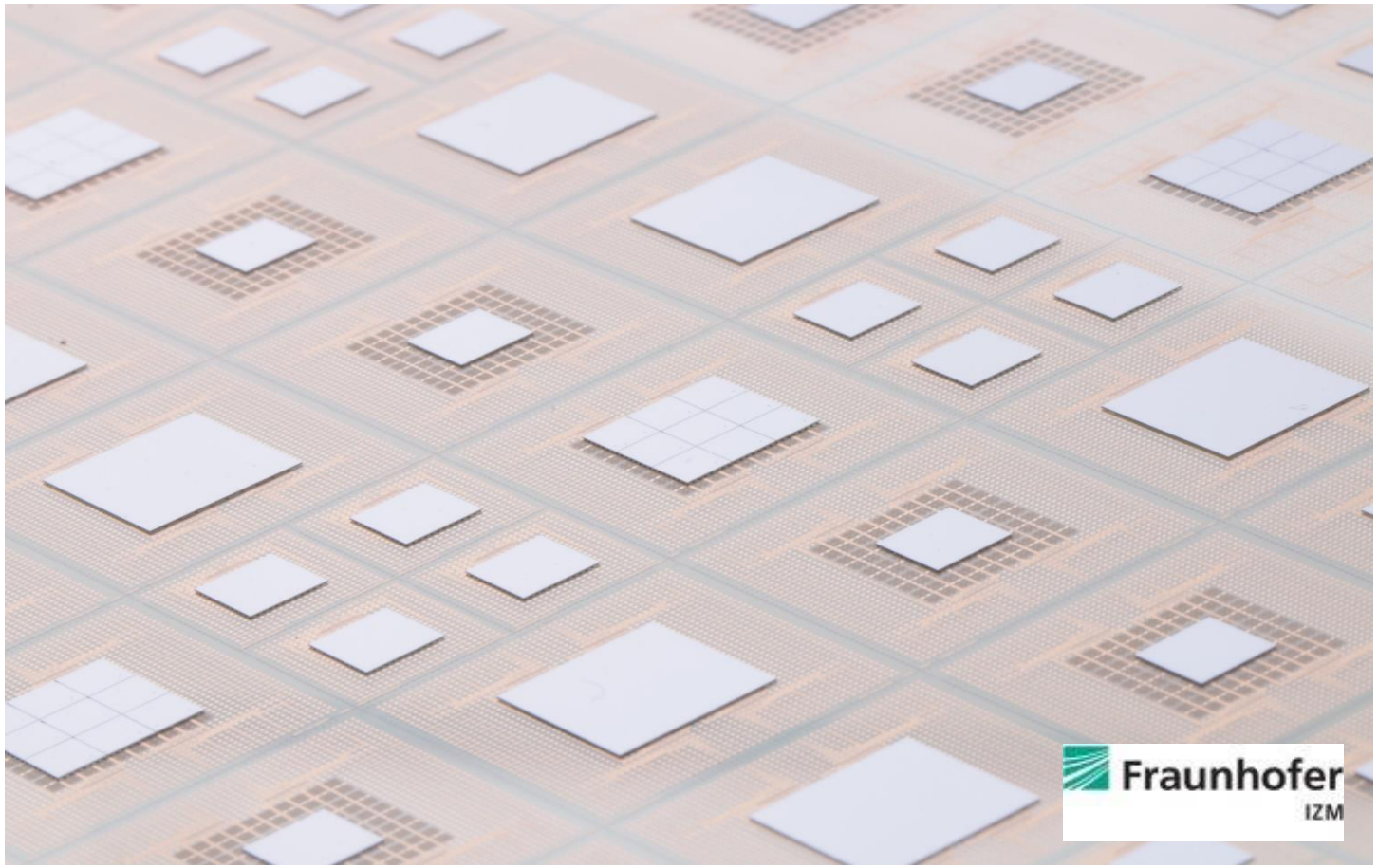
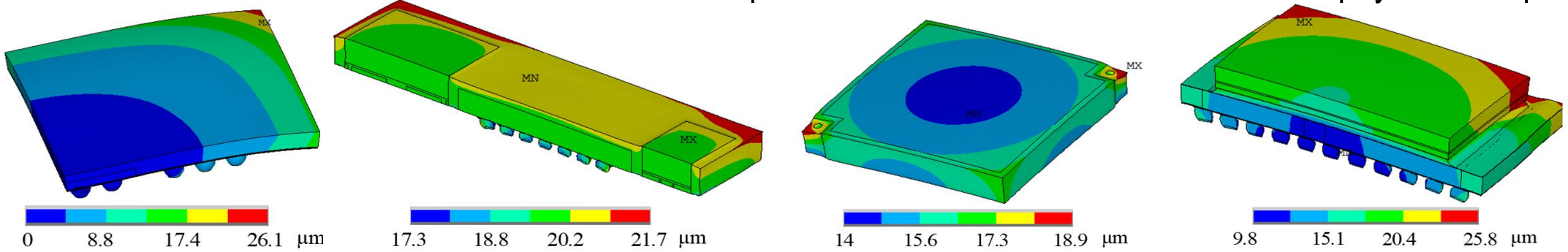


Figure 1. An example of a new test design developed in EuroPAT-MASIP project for two package dimensions 10mm x 10mm
and 20mm x 20mm to be used for next generation fine-pitch FO-WLPs.

An example of simulation results: Universal design for reliability platform for all FO-WLP products

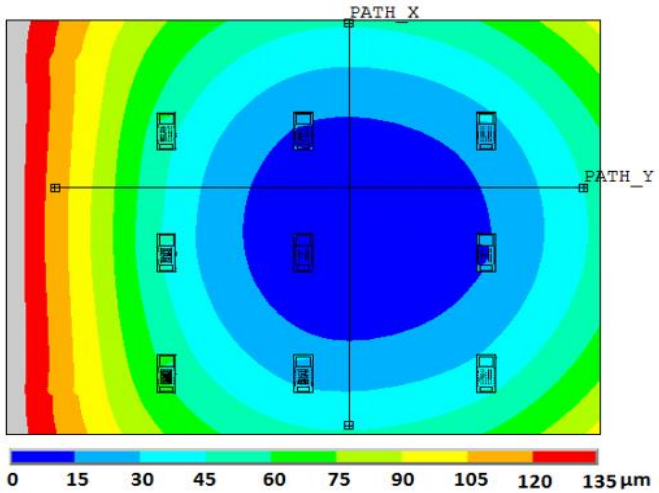
Simulation Prediction: Warpage at -40°C after Thermal Cycles for all Package Types

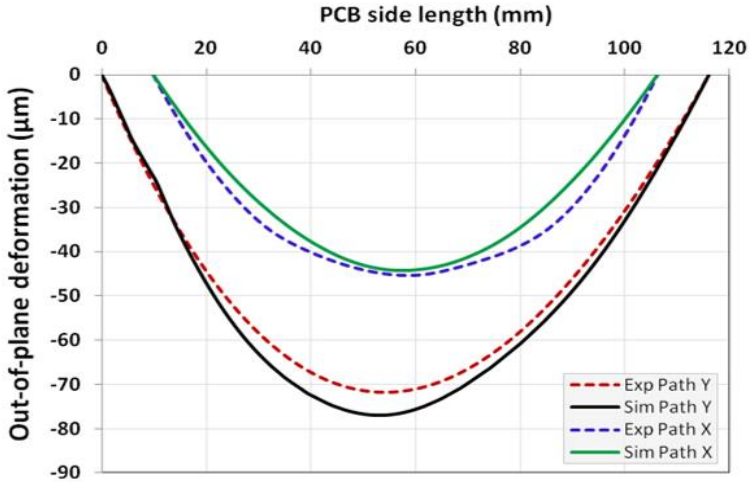
Parametric models enable the assessment of all future products before the fabrication of the first physical samples



Single Die Package Multi Die System in Package

Validation: Perfect Match – Board & Component Warpage – Simulation & Experiment





Fraunhofer ENAS

An example of demo results: AP#6 WLAN Front-End IC

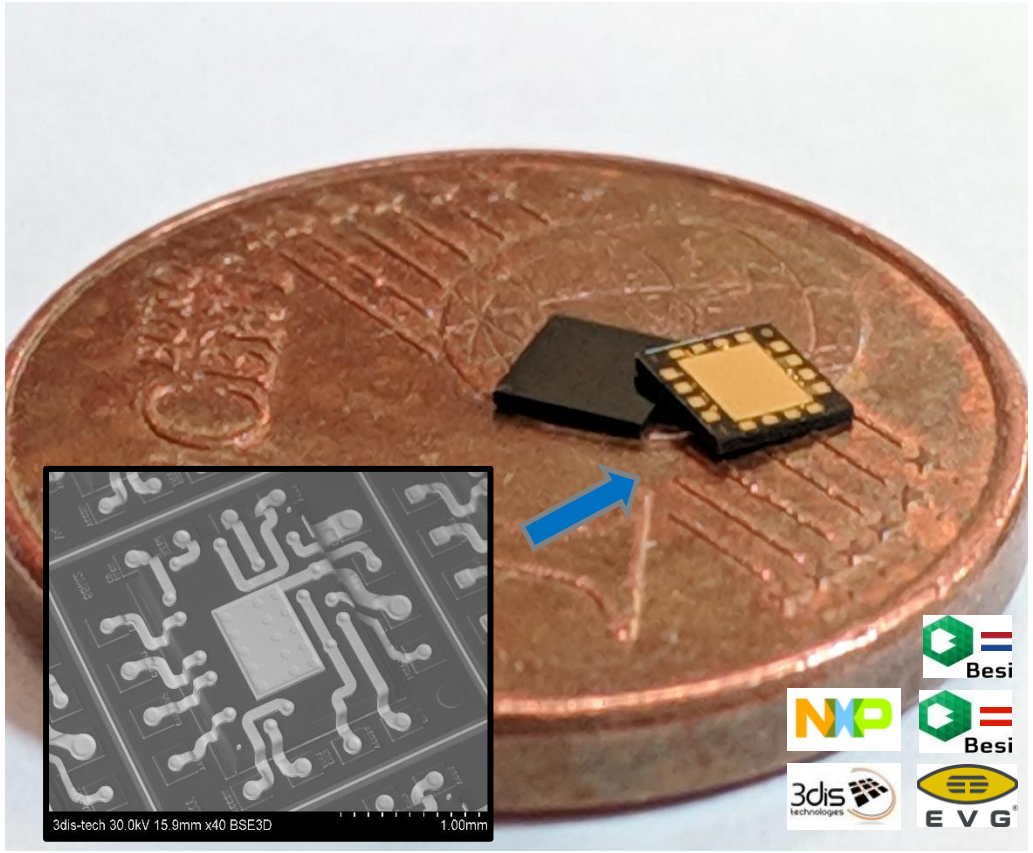


Figure 2. A packaged device of the first prototype for WLAN Front-End IC (Application Pilot #6 owned by NXP FR in EuroPAT-MASiP project).

An example of process and technology development results: Self-alignment and Pick & Place

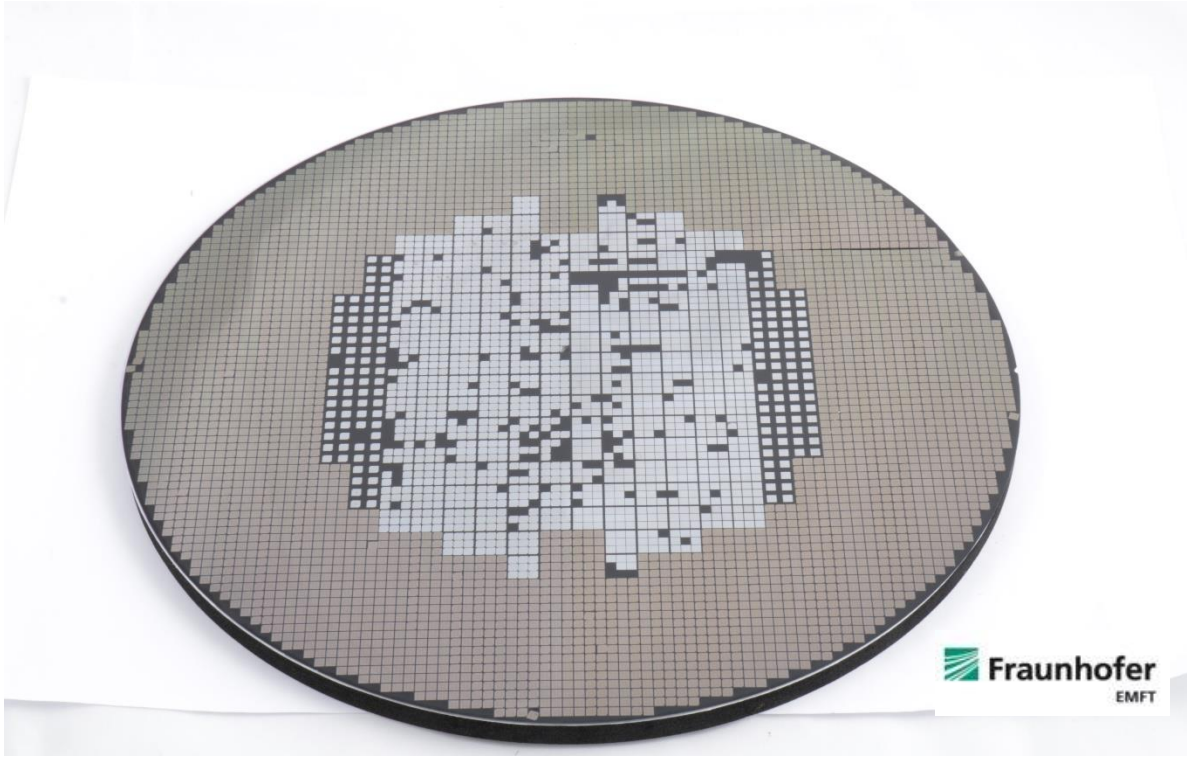


Figure 3. Reconstruction wafer with transferred chips in the middle (arranged by self-alignment process) and chips in the outer area populated by standard pick & place process in EuroPAT-MASiP project.


F2F meeting
Innsbruck 12.2.2019

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https://www.europat-masip.eu/news/