EuroPAT MASIP

Research results highlights

Update: November 2020



This project has received funding from the ECSEL Joint Undertaking under grant agreement No 737497. This Joint Undertaking receives support from the European Union's Horizon 2020 research and innovation programme and Portugal, Austria, Netherlands, Finland, Germany, Hungary, Ireland, France, Sweden

Reseach in EuroPAT-MASIP

Research in EuroPAT-MASIP project focuses on improving the manufacturing of advanced packaging technologies, mainly Fan-Out Wafer-Level Packaging (FO-WLP/WLFO) and Embedding Technologies towards 2D and 3D System Integration.

- All the following results have already been published and presented in a conference or industry event
- To find the original articles, please check the links provided on slides or visit our website at https://www.europat-masip.eu/publications-events/





FO-WLP Multi-DOF Inertial Sensor for Automotive Applications

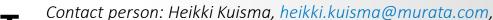
Two MEMS dies (gyroscope, 3-axis accelerometer) were combined with an integrated circuit in FOWLP package.

RESULTS: Three failure modes were identified (black pad due to Ni finish of the PCB; solder fatigue at very early stage; copper RDL fracture at the boundary of the solder ball and free RDL metallization). However, solder fatigue was no issue and by design changes two other mechanisms can be corrected.

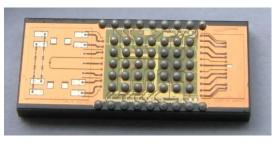
MOTIVATION: FO-WLP allows multi-die packaging with minimum package dimensions: this is needed in automotive applications as the amount of sensors is increasing but the physical space on control boards is not.

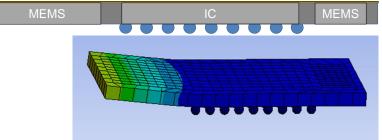
IMPACT/APPLICATION: The research shows that FO-WLP will reach **automotive reliability requirements** by passing high temperature, thermal cycle and temperature-humidity tests.

https://ieeexplore.ieee.org/document/8546447





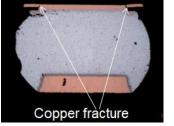
















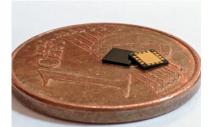


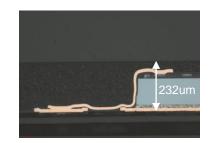


Ultra-thin QFN-Like 3D Package with 3D Integrated Passive Devices

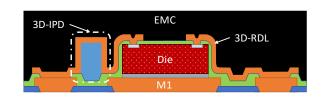
- A novel 3D-RDL-based Ultra-thin QFN-like 3D Wafer-Level package with integrated passive device was successfully developed and demonstrated
- Target was to achieve a total package thickness of 200µm with a package configuration that allows good electrical and thermal performance
- Packaging process required accurate die bonding, low bleed of CDAF, high aspect-ratio, high resolution
 3D-RDL, thin cap overmolding and laser debonding
- A placement accuracy of 3μm 3σ and a bleeding distance < 6μm were obtained
- Conformal 3D-RDL with 15 μm L/S over 170um tall step and via opening
 17.5μm over 3D topology were achieved
- · Low-temperature, defect-free laser debonding and cleaning was obtained
- Overmolding of 3D topology with a resulting 35μm-thin cap over the die and a total package thickness of 230μm
- Technology was successfully demonstrated to package a WLAN RF Frontend die and to form High-Q 3D inductors

Contact person: Ayad Ghannam, ayad.ghannam@3dis-tech.com



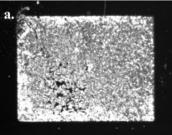


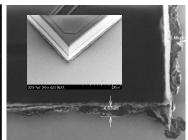
Cross-section of overmolded package

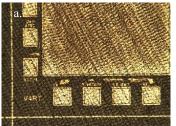


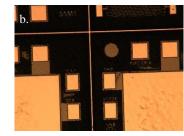
Good DAF wetting

Small DAF bleeding distance

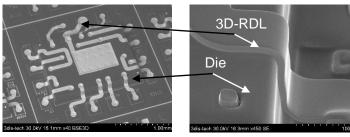








Laser debonding before and after cleaning using NMP



SEM images of integrated package before molding





Automated Virtual Prototyping for Fastest Time-to-Market of New System in Package Solutions



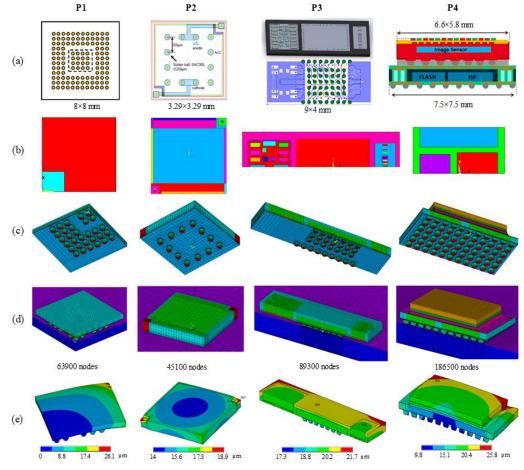
RESULT: A modular system of parametric FE models is created using ANSYS for automated virtual prototyping of current and future System-in-Package (SiP) solutions based on fan-out-wafer-level-packaging (FO-WLP) technologies.

MOTIVATION: Creation of virtual prototyping scheme to shorten time-to-market, to explore a wide range of design alternatives using Design of Experiments (DoE) and optimize products for improved performance and reliability

APPLICATIONS/IMPACT: Virtual prototyping has allowed to study four demonstrator packages with different structures.

Contact person(s): Ghanshyam Gadhiya, <u>ghanshyam.gadhiya@enas.fraunhofer.de</u>
Sven Rzepka, <u>sven.rzepka@enas.fraunhofer.de</u>

https://ieeexplore.ieee.org/document/8546352



Demonstrator packages (a) schematic, (b) package areas created using parametric area modeling step, (c) FE models without substrate, (d) FE models with substrate mentioning nodes and (e) warpage at -40°C after 2.5 thermal cycles





The Creation of a Validated Scheme for the Automated Optimization of Systems in Package Designs

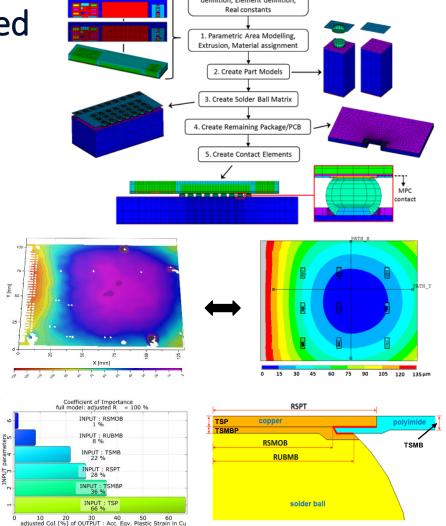
RESULT: A method is presented to create a validated scheme for the virtual prototyping of an automotive inertial sensor involving the material characterization, warpage measurement, finite element analyses validation and sensitivity analysis.

MOTIVATION: Study the reliability influence of different design variations of solder ball pad structure of fan-out packages using virtual prototyping schemes incorporating validated FE model.

APPLICATIONS/IMPACT: Virtual prototyping has allowed to study a optimum pad design to prevent pad cracks and solder ball fatigue leading to improved reliability.

Contact person(s): Ghanshyam Gadhiya, <u>ghanshyam.gadhiya@enas.fraunhofer.de</u>
Heikki Kuisma, heikki.kuisma@murata.com

https://ieeexplore.ieee.org/abstract/document/8727787











Towards improved FO-WLP manufacturing by using selfalignment process

RESULT

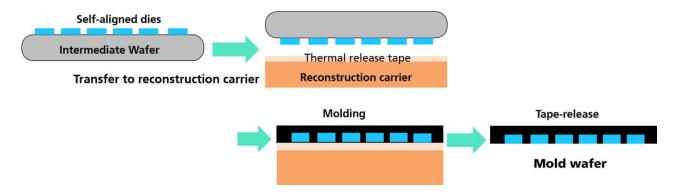
Self-alignment of dies in the context of a total FOWLP process **was demonstrated** successfully with accuracy having the potential **to outperform standard pick & place**.



MOTIVATION

Improving the manufacturing process chain:

- Plasma treatment of the intermediate carrier wafer
- Dispensing of assembly liquid onto target areas
- Pick & place of dies without contacting target areas



FOWLP with self-alignment process

APPLICATIONS/IMPACT

Future developments focus on the potential of self-alignment to increase assembly throughput (UPH) drastically by implementing multi-die handling tools. This makes self-alignment a promising approach in FOWLP manufacturing.









Assessment of FO-WLP process dependent wafer warpage using parametric FE study

RESULT: The wafer warpage studies revealed that:

- ✓ The 300 mm diameter thin wafer shows highly nonlinear behavior.
- ✓ Reconstituted wafer shows bifurcation behavior.
- ✓ FOWLP process induced warpage is replicated using FE analysis.
- ✓ The gravitational force has significant effect on the wafer warpage.

MOTIVATION: Study of excessive wafer warpage which is still a crucial challenge for the Fan-out technologies often impeding the subsequent processing steps and results in total loss of wafers.

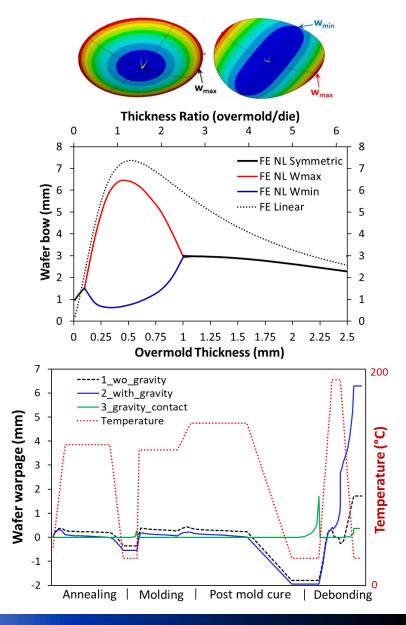
APPLICATIONS/IMPACT: Study is used by partner to understand and optimize the wafer warpage during processing steps.

Contact person(s): Ghanshyam Gadhiya, <u>ghanshyam.gadhiya@enas.fraunhofer.de</u>

Sven Rzepka, <u>sven.rzepka@enas.fraunhofer.de</u>

https://ieeexplore.ieee.org/document/8951805









Virtual Prototyping, Design for Reliability, and Qualification for a Full SiP Product Portfolio of a FO-WLP Line

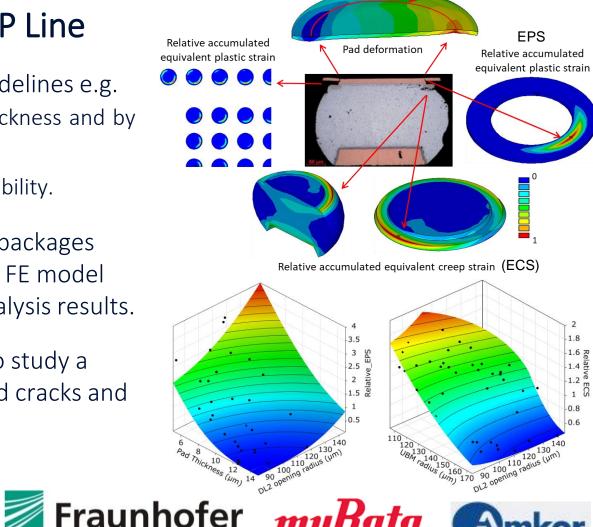
RESULT: The virtual DoE studies revealed many design guidelines e.g.

- ✓ Pad lifetime could be increased by increasing the pad thickness and by decreasing DL2 opening diameter.
- ✓ UBM diameter has strong influence on the solder ball reliability.

MOTIVATION: Study of different failure modes of fan-out packages using virtual prototyping schemes incorporating validated FE model using qualitative match with measurement and failure analysis results.

APPLICATIONS/IMPACT: Virtual prototyping has allowed to study a new RDL pad structure with undulations incorporating pad cracks and delamination leading to improved patent application.

Contact person(s): Ghanshyam Gadhiya, <u>ghanshyam.gadhiya@enas.fraunhofer.de</u>
Heikki Kuisma, <u>heikki.kuisma@murata.com</u>



periphery = crack path

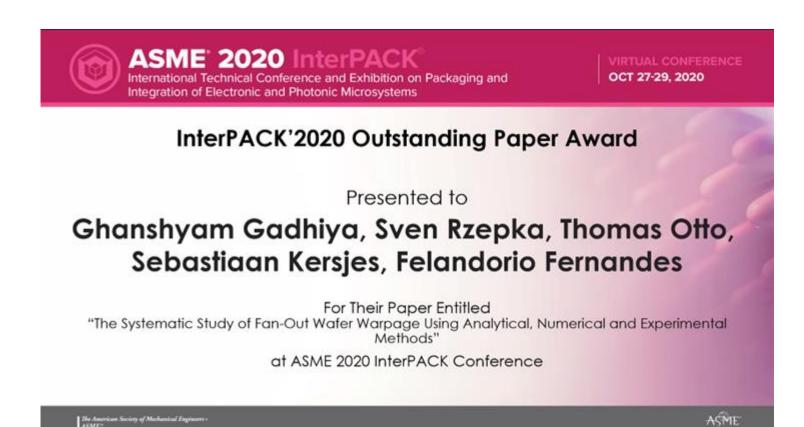






ASME InterPACK'2020 Oustanding paper award

Learn more about this latest award-winning paper by visiting our booth at EFECS!









Visit our website for latest news and results!

https://www.europat-masip.eu/news/

