# Chip Package Bumping on Wafer-level for RDL First Fan-out Wafers

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## Abstract

Advanced chip technologies need package solutions with a chip/package interface that reaches electrical performance needs, allows proper heat dissipation and reaches needed reliability constraints. To address further demand, this development aims at modifying the current solder bumping tool for handling warped/ thin wafer and also to reduce the overall chip height to enable increased packing density. Solder bumping i.e., forming the solder bumps for I/Os of the chip packages are to be developed for wafer level for thin and warped wafer. It also requires modifications of equipment as well as developing/optimizing the processes for chip package bumping on wafer level. A solder bumping process of RDL first fan-out molded wafers is evaluated at the wafer-level in this work and the handling challenges faced during these evaluations are explained. A good solder placement process could be observed on the Fan-Out wafers; but a following oven reflow process was quite challenging. A laser scanned reflow on localized pads helped to overcome the constraints.

## Key words

Wafer-level bumping, Fan-Out wafer level packaging, RDL-1st packaging, Epoxy molded compounds, Redistribution layer, Laser reflow.

## I. Introduction

Fan-out wafer-level packaging (FOWLP) is one of the most attractive advanced packaging trends in microelectronics since it allows an improved form factor with reduced package volume and package thickness. Moving to an era of System-in-Package (SiP) and heterogeneous integration, FOWLP is an increasingly important packaging approach [1]. FOWLP also enables better thermal packaging performance with a shorter heat dissipation path from the die to the printed circuit board (PCB). FOWLP combines multiple chips from heterogeneous processes into a compact package, thereby reducing the footprint [2]. Chips (also known as known good dies or KGD) are embedded in an epoxy molded compound (EMC) and then a metal redistribution layer (RDL) establishes the connections within the package without any need of Through Silicon Vias (TSVs) or a laminate package substrate. In an RDL first approach, RDL layers are built-up on a carrier wafer and known good dies are attached to the RDL followed by the molding process and solder bumping. Wafer handling challenges appear after epoxy molding that leads to warpage of the molded wafer due to the coefficient of thermal expansion (CTE) mismatch between silicon (Si) and the mold compound. In this work, a solder bumping process of RDL first fan-out molded wafers are evaluated at the wafer-level and the handling challenges faced during these evaluations are explained.

## II. Results and discussion

*A. Process Flow:*

Detailed schematics of process flow of RDL first Fan-Out wafer fabrication is shown in Fig. 1.

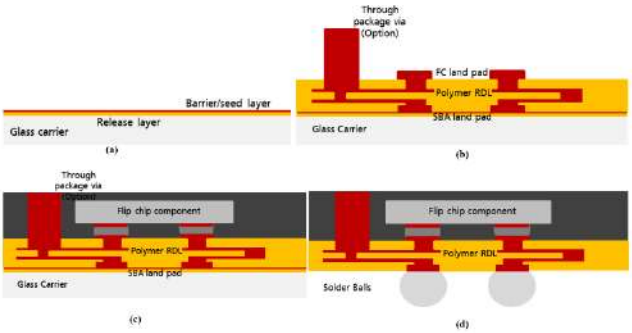


Fig. 1: Schematics of complete RDL first process flow of Fan-Out wafer fabrication.

As first step the application of release layer on temporary glass carrier followed by deposition of barrier/ seed/ protection layer is carried out as shown in Fig. 1(a). A sequential build-up of a multilayer polymer RDL (in Fig. 1(b)) is performed to fabricate:

- Land pads for solder ball attach (SBA)
- Multi-layer copper redistribution layer for fan-out and component to component wiring
- Land pads for flip chip assembly as well as IPD assembly
- Through package via (TPV) for top to bottom interconnects

Next steps are the die to wafer assembly of flip chip components and mass solder reflow, wafer mold by injection molding including mold underfill, TPV open by modified molding process and/or mechanical back grinding (shown in Fig. 1(c)) and laser release of temporary glass carrier and post laser release cleaning steps to remove of release layer residues, wet etch of temporary barrier/ seed/ protection layer. Cleaning of SBA land pads, application and reflow of solder balls (as shown in Fig. 1(d)).

*B. RDL design:*

For proving the RDL-1st packaging concept, a generic test design covering RDL-1st substrate as well as a flip chip wafer with daisy chain pattern were developed. The concept allows the application of dies in the range from 1mm x 1mm up to 10 mm x 10 mm. It also allows a multi die placement inside a package. Daisy chains are implemented to measure the interconnects between chip and RDL-1st substrate, between solder ball and after assembly between board and die to characterize electrical parameter after fabrication and aging.

A generic daisy chain design has been developed for proving the RDL-1st concept. Line/space of 10 µm/10 µm was chosen as basic design rule. To demonstrate high density wiring capability, the application of 5 µm line/space as well as 2 µm line/space were investigated. Line/space of 2 µm, tall Cu-Pillar and different IPD designs have been implemented, as shown in Fig. 2.

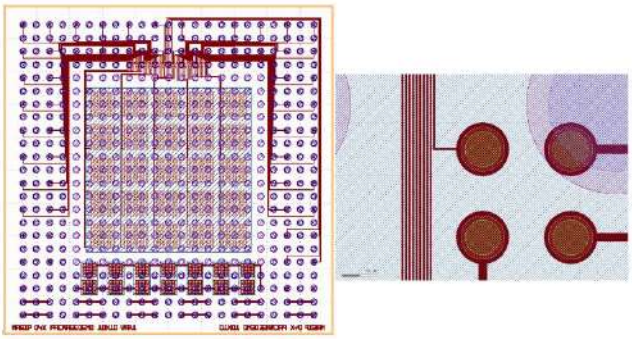

Fig. 2: Generic daisy chain design showing (a) dense RDL area, FC µ-pillar, test and IPD pads; (b) details of 2 µm line/space RDL inside the die area.

The access for electrical measurements of the daisy chains is via test pads, via SBA-Land pads and even by using the tall Cu-pillar from the top side of the package. To support high density wiring new resist material for RDL patterning was introduced and the wet etch steps for UBM removal has been adjusted. The undercut of the RDL-lines was measured below 100 nm, typically below 50 nm. Both modifications are required for further reduction of line/ space to 2 µm.

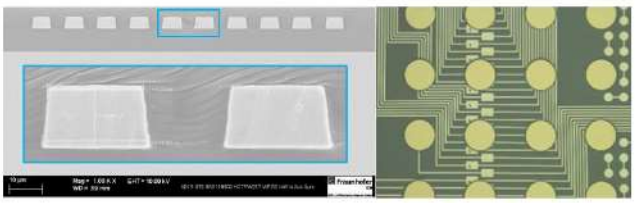

Fig. 3: (a) RDL cross-section through high density copper-RDL, 5 µm line/space, 3 µm thick; (b) Top view of multi-layer RDL showing SBA-land pads, test pads, RDL and FC-land pads.

The cross-section through the high-density wiring areas (Fig. 3a) refers to a 5 µm RDL line/space. The thickness of the RDL is around 3 µm. The top view shows all metal pattern of the RDL-1st after removal from the glass carrier.

Fig. 4 depicts the wafer pictures after DC chips assembly and after molding process.

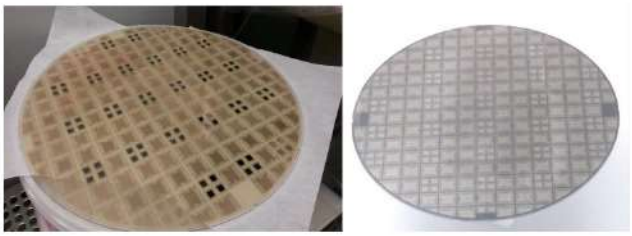

Fig. 4: (a) RDL 1st test wafers after DC chips assembly; (b): after molding process.

*C. Molding Process:*

The wafer level transfer molding on the RDL first wafers is performed on a commercially available Besi FML molding system. In this system, the EMC is transferred inside the cavity after the mold tool is closed. Thereby differing significantly from the more standard compression molding. This approach has some specific advantages in cost reduction by using standard pelletized EMC's and integration strategies by the ability to keep areas exposed [3]. For this sample build the handling and processing is done manually, but other Besi tools perform this step automatically.

Before molding the wafer with RDL layer was plasma activated using an $ArH_2$ plasma (300 w). After this, the wafer is loaded inside the mold tool and gently clamped, Fig. 5a. A 50 µm thick PET foil is fixated to the inner surfaces of the mold to protect it from the transferred EMC. During EMC transfer Fig. 5b, the pressure between the sample and the mold is kept constant, by a dynamic clamp force control (DCC [4]), preventing any damage to the wafer. Moreover, the injection speed is controlled to smoothly fill the mold with a transfer speed starting at 5 mm/s, slowing down to 2 mm/s and lower. The molding tool is equipped with a venting mechanism that mechanically closes as soon as the cavity is completely filled. After that, the temperature (175°C) and the pressure (7 MPa) are kept constant for the time needed for pre-curing of the EMC (7 min). After curing, Fig. 5c, the molding press opens and the molded wafer is removed. Finally, the wafer is post mold cured for 4hrs at 175°C.


Fig. 5: Schematic process flow of the RDL-1st FO-WLP transfer molding process.

*D. Bumping Process:*

Bumping machine capability for handling warped wafers shows successful handling of wafer warpage of ~3 mm for dummy wafers. The bumping process evaluation was carried out on real wafers with warpage <1 mm. Handling real wafers during the bumping process is critical since the epoxy molded wafers are like 'paper' after release from the glass carrier. A seed layer etching step was carried out to etch Ti and Cu seed layer before solder bumping process. A new process optimization has to be carried out as the wafers are thin and was not possible to do the handling in etching chemicals without a backside tape support. A short $O_2$ plasma step before etching helped to remove the metal layers completely from the wafer.

Bumping evaluations on wafer level were carried out using PacTech's Ultra-$SB^2$ machine; in which the bond-head picks (turning on vacuum) solder balls from reservoir to a stencil (Fig. 6(a)) followed by removal of excess solder balls by ultra-sonic and optical inspection of the stencil (Fig. 6(b)) and placement of the balls on a pre-fluxed wafer (Fig. 6(c)). Fig. 6(d) shows a schematic of the ball placement process on a pre-fluxed wafer. After placement of the solder spheres on the wafer, a reflow process is followed to create good adhesive bonding of the balls to the pads.

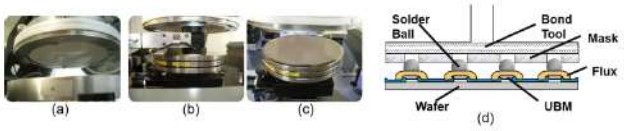


Fig. 6: Wafer level solder ball placement by using a stencil; (a) vacuum picking of solder balls from reservoir, (b) removal of excess balls & optical inspection and (c) placement of solder balls on the wafer; (d) schematic showing the ball placement.

The solder bumping process was carried out as a ball drop on flux process in which solder balls of a lead-free solder alloy, tin-silver-copper (SAC305), are placed from a reservoir through a stencil onto an already flux-printed pad surface; a subsequent reflow step is needed to confirm bonding of the solder balls to the pads. Flux printing and ball placement are done using a stencil and a following reflow process. Placement of solder spheres on these molded wafers looked quite promising. Fig. 7(b) and (c) show pictures of wafer after flux printing and solder ball placement processes. The wafers were mounted on a reflow-compatible backside tape; but even with backside support it was not possible to handle the wafers after ball placement as the wafers look like a 'paper'. A picture of the wafer without backside tape is

shown in Fig. 7(a). Wafers were glued to Si dummy wafers for better handling during the process.

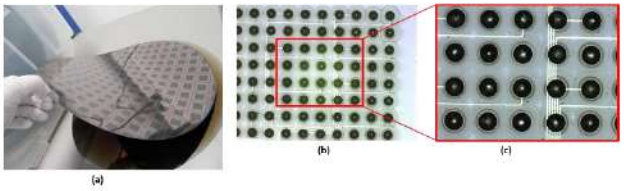


Fig. 7: (a) Picture showing the wafer after removing from the backside tape. Handling w/o carrier is complicated due to the "paper-like" nature of the wafers. (b) Image of the wafer surface after ball placement process using flux printing but before reflow. Solder Ball placement on these molded wafers look quite promising.

Performing a reflow process on molded wafers is quite challenging due to the mechanical stress generated at the high temperature used for reflow, which may influence the performance of the device. Mechanical stress and deformation of the molded wafer is observed due to the mold compound shrinkage at high temperature and thermal expansion differences between the chip and mold compound. Again, processing FOWLP wafers during solder reflow to a peak temperature of ~250°C is critical due to their thermal fragility. A low temperature solder process can be tried using low melting temperature solder alloys like indium-tin (In-Sn) or indium-bismuth (In-Bi), but this limits many operations on the device. Reflow inside an oven shows discoloration of the epoxy mold material as the required reflow temperature for the solder alloy (SAC305) is 250°C and a very high wafer warpage was observed leading to high risk of wafer breakage. A laser reflow helps to overcome this problem; which involves localized reflow on the pads by laser scanning. PacTech`s LaPlace system is used for this purpose with a laser pulse of 500 ms and the measured temperature at this pulse is 250°C. Mechanical test with a jaw and shear test of the reflowed bumps shows a good adhesive bonding of the solder balls to the bumped bondpads; with an average shear force value of 150 g for 200 µm pads. An SEM picture of the wafer surface after complete solder bumping process is shown in Fig. 8.

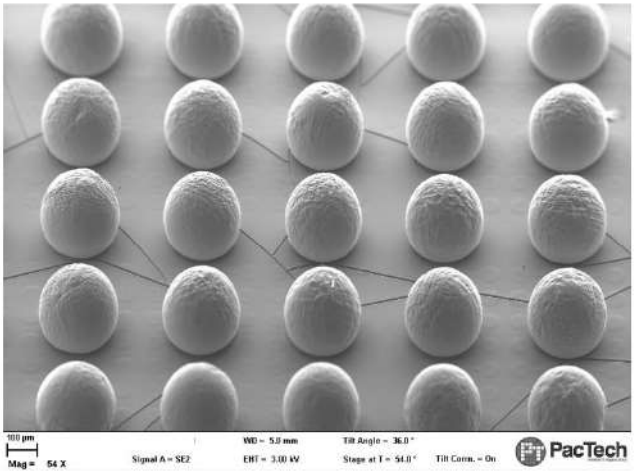


Fig. 8: SEM image of wafer surface after solder bumping process.

## III. Conclusion

A process flow for proving RDL-1st Fan-Out packaging concept is established. High density Cu RDL with 5µm line/space is used for this. A solder bumping process of RDL first fan-out molded wafers is evaluated at the wafer-level in this work and the handling challenges faced during these evaluations are explained. A good solder placement process could be observed on the Fan-Out wafers; but a following oven reflow process was quite challenging. A laser scanned reflow on localized pads helped to overcome the constraints.

## Acknowledgment

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